# A Two-Loop Feedback Control Strategy For Neutral Point Voltage Balancing Of Vienna Rectifier With A Carrier-Based Implementation

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***Abstract*—Neutral point voltage unbalancing is one of the key issues faced by Vienna rectifier, which causes line current distortion, higher device stress, and eventual failure. This unbalancing is caused by the neutral point current which is a function of modulation strategy. The distribution of the dwell time of a space-vector between its redundant switching states impacts this neutral point current. But the model between the neutral point voltage and the distribution factor is non-linear. Therefore, the existing control strategy based on the small-signal linearized plant is not effective to mitigate the unbalance. This paper proposes an alternative control strategy where the plant becomes linear under large-signal variation. Hence, a simple controller can balance the neutral point voltage on a cycle-by-cycle basis. It also nullifies the DC offset across the capacitors during start or transient. A carrier comparison based implementation of the proposed control is also proposed. The proposed strategy is verified through simulation and experiment on a 1 kW hardware prototype.**

***Index Terms*—Nearest three space-vector PWM, Carrier-based implementation**

## I. Introduction

EVER since the introduction of the Vienna Rectifier (VR) in 1994, it gained popularity as a suitable candidate for applications like power factor correction (PFC) [1], telecom rectifier [2] etc. Similar to three-level converter, VR also has following advantages over two-level rectifier- reduced dv/dt stress, lower high-frequency voltage ripple and hence, smaller filter size, higher voltage handling capability. However, neutral point voltage balancing is one of the key challenges present in VR. This work presents a closed-loop control strategy to balance mitigate this issue and its carrier-based implementation is also shown.

The DC-bus of VR consists of two identical series-connected capacitors, which provide a split DC voltage output with respect to a neutral point. The voltage mismatch between these capacitors is known as neutral point voltage unbalancing. This mismatch is caused due to non-zero neutral point current, which is impacted by the modulation strategy of VR. Although the number of switching states of VR (8) is much smaller than switching states of three-level converter (27), the modulation strategy of VR is similar to one of the very common modulation strategies of three-level converter, namely, nearest three vector PWM scheme (NPWM), [3], [4]. Here, the reference voltage vector is synthesized using three adjacent vectors. One of the three nearest vectors can be realized with two redundant states. Equal distribution of dwell time among these two states results in so-called Conventional NPWM (CNPWM), [5]. Although the implementation of CNPWM is simple, [5], but it results in significant voltage ripple across the capacitors of frequency three times of line frequency, [6], [7]. Optimal distribution of dwell time among the redundant states can minimize the capacitor voltage ripple, [8], which is known as General NPWM (GNPWM) scheme. Using the higher number of switching states, three-level inverter solves this problem using Virtual space-vector PWM (VPWM), Special three space-vector PWM (S3PWM), [9], [10]. Implementation of these schemes is difficult and not possible for VR as the number of states is limited.

[6], [11], proposed a closed-loop control scheme to determine the optimal dwell-time distribution factor of GNPWM scheme to solve the neutral-point unbalancing problem. The plant model is non-linear and changes with operating condition. Therefore, designing of controller to achieve certain performance specification is difficult. Moreover, the voltage ripple couldn't be made zero because of the small-signal nature of the plant. This paper proposes an alternative control strategy to solve these issues. The proposed model of the plant is linear, large-signal valid and exact. Therefore, any kind of dynamic unbalancing of neutral point voltage as well as DC offset can be mitigated through the proposed controller. Through a proposed two-loop control architecture-the faster loop eliminates the third-harmonic voltage ripple, whereas the slower loop rectifies any initial or transient DC offset. The paper further shows a simplified carrier-comparison-based implementation of the proposed control architecture.

The organization of the rest of the paper is as follows- Section II elaborates the modelling of $3\phi$ VR and its modulation strategy; Section III highlights the neutral point voltage unbalance in VR and neutral point voltage unbalancing of VR and the proposed control strategy to mitigate this. A carrier-based implementation is shown in section IV; Section V validates the proposed algorithm through both simulation and experimental results. Finally, Section VI concludes the paper.

## II. Modulation Strategy of Vienna Rectifier

### A. Modelling Of VR

Fig. 1(a) shows the circuit diagram of a three-phase VR. The pole point, $X$, of each phase is connected to the positive and negative DC buses (of DC-bus voltage $V_{dc}$) through diodes $D_{XP}$ and $D_{XN}$, respectively, where $X \in \{A, B, C\}$. Two identical capacitors, $C_P$ and $C_N$), are connected in series across the DC-bus of VR. The DC-bus midpoint, $N$, is connected to pole point $X$ with one four-quadrant switch, $S'_X$. One way of realizing the four-quadrant switch is indicated in Fig. 1(a). This VR is connected to a three-phase AC source with a inductor (filter circuit) connected between the source and the pole point. Three phase voltages are denoted by $V_{gA}$, $V_{gB}$, and $V_{gC}$, respectively; $L$ is the value of the inductor connected between the source and VR.

Each controllable switch, $S'_X$, has two states, .viz, 'ON' (denoted by '1') and 'OFF' (denoted by '0'). As there are three such controlled switches in VR, the converter has $2^3 = 8$ switching states. The labelling of these states are given in Table I. Each of these states are denoted by three binary numbers in succession, which denote the 'ON' or 'OFF' states of $S'_A$, $S'_B$, and $S'_C$, respectively. For example, state 010 denotes $S'_A$, $S'_C$ are 'OFF' and $S'_B$ is 'ON'. The pole voltage, $v_{XN}$, of $X^{th}$-phase of VR depends upon both state of $S'_X$ and the current polarity of $i_X$. If $S'_X$ is 'ON', $v_{XN} = 0$. When $S'_X$ is 'OFF', either $D_{XP}$ or $D_{XN}$ comes in conduction based on the polarity of $i_X$. Hence, $v_{XN}$ will be either $+\frac{V_{dc}}{2}$, or $-\frac{V_{dc}}{2}$. The generalized pole voltage equation is given in (1), where $G_X$ denotes the state of $S'_X$.

$$v_{XN} = \frac{V_{dc}}{2}(1 - G_X)\text{sign}(i_X) \tag{1a}$$

$$\text{sign}(i_X) = \begin{cases} +1 & i_X \geq 0 \\ -1 & i_X < 0 \end{cases} \tag{1b}$$

$$G_X = \begin{cases} 1 & S'_X \text{ 'ON'} \\ 0 & S'_X \text{ 'OFF'} \end{cases} \tag{1c}$$

Therefore, the modeling of switching states of VR depends upon the position of the reference current vector, $\vec{i}_{ref}$, where $\vec{i}_{ref}$ is obtained from the phase currents using Clarke's $A - B - C$ to $\alpha - \beta$ transformation, as shown in (2).

$$\vec{i}_{ref} \triangleq i_\alpha + j i_\beta = \frac{2}{3}\left(i_A e^{j0} + i_B e^{j\frac{2}{3}\pi} + i_C e^{j\frac{4}{3}\pi}\right) \tag{2}$$

Based on the directions of $i_A$, $i_B$, and $i_C$, the $\alpha - \beta$ plane can be divided into six regions, called as current sector (CS). Fig. 2 shows these six sectors, CS-1 to CS-6, and the corresponding current directions are mentioned in each sector.

For $\vec{i}_{ref}$ belongs to any given CS, one can find the pole voltages, $v_{XN}, X \in \{A, B, C\}$, of the 8 switching states using (1), and thereafter find the corresponding voltage space-vectors using (3).

$$v_\alpha + j v_\beta = \frac{2}{3}\left(v_{AN} e^{j0} + v_{BN} e^{j\frac{2}{3}\pi} + v_{C_N} e^{j\frac{4}{3}\pi}\right) \tag{3}$$

Let's consider a case for an example, where $\vec{i}_{ref}$ belongs to CS-1 (shown in Fig. 2), hence, $i_A > 0, i_B < 0, i_C < 0$. The space-vectors generated by the eight switching states in CS-1 are indicated in Fig. 3. Here, the vector lengths are scaled by $\frac{1}{V_{dc}}$. Let's consider 000 state, where all the three switches are 'OFF'. With the given current directions, $v_{AN}$, $v_{BN}$ and $v_{C_N}$ are determined from (1) as $v_{AN} = +\frac{V_{dc}}{2}$, $v_{BN} = -\frac{V_{dc}}{2}$, $v_{C_N} = -\frac{V_{dc}}{2}$. Substituting these pole voltages in (3) give space vector of $\frac{2}{3}V_{dc}e^{j0}$. This space vector is shown in Fig. 3 after scaling by $\frac{1}{V_{dc}}$. Other switching states can also be mapped in the similar way. These states give six active voltage vectors and one zero vector in $\alpha - \beta$ plane. Two states, 011 and 100, give the same active vector, hence, there are two redundant states corresponding to one active vector. In a similar manner, one can map the space-vectors for all six current sectors, as shown in Fig. 2. These voltage vectors, eighteen distinct active vectors and one zero vector, are same as the vectors generated by a three-level converter, [6].

TABLE I: SWITCHING STATES

| State | $S'_A$ $S'_B$ $S'_C$ | State | $S'_A$ $S'_B$ $S'_C$ |
|---|---|---|---|
| 000 | OFF OFF OFF | 100 | ON OFF OFF |
| 001 | OFF OFF ON | 101 | ON OFF ON |
| 010 | OFF ON OFF | 110 | ON ON OFF |
| 011 | OFF ON ON | 111 | ON ON ON |

### B. Modulation Strategy

When Clarke's transformation is applied on the average line-neutral voltages, $\bar{v}_{AN}$, $\bar{v}_{BN}$, and $\bar{v}_{CN}$, which are desired to be synthesized over one carrier cycle, the reference voltage vector, $\vec{V}_{ref}$, is obtained as shown in (4a). Here $\bar{v}_{XN}$ is the average of $v_{XN}$ over a carrier period, $T_{sw}$. As the space-vectors in Fig. 3 and Fig. 2 are per-unitized by $V_{dc}$, $\vec{V}_{ref}$ is also normalized with respect to $V_{dc}$ in (4b) to make the analysis independent of DC-bus voltage. Here, $m_X \triangleq \frac{\bar{v}_{XN}}{V_{dc}}, X \in \{A, B, C\}$ and $\vec{m}_{ref} \triangleq \frac{\vec{V}_{ref}}{V_{dc}}$.

$$\vec{V}_{ref} \triangleq \bar{v}_\alpha + j\bar{v}_\beta = \frac{2}{3}[\bar{v}_{AN}e^{j0} + \bar{v}_{BN}e^{j\frac{2}{3}\pi} + \bar{v}_{CN}e^{j\frac{4}{3}\pi}] \tag{4a}$$

$$\vec{m}_{ref} = \frac{2}{3}[m_A e^{j0} + m_B e^{j\frac{2}{3}\pi} + m_C e^{j\frac{4}{3}\pi}] \tag{4b}$$

As VR operates at unity power factor, the voltage and current vectors are in same phase. Therefore, for $\vec{i}_{ref}$ belongs to CS-1 (spans $-30^\circ$ to $30^\circ$ of $\alpha - \beta$ plane), the corresponding $\vec{m}_{ref}$ will also lie within the same angular span, as indicated in Fig. 3. Here, the modulation strategy, i.e., the synthesis of $\vec{m}_{ref}$, in CS-1 using the eight switching states of VR is discussed. The same strategy can be extended for other current sectors.

The Nearest Three Vector (NTV) strategy is the most popular modulation strategy for VR and the three-level inverter, [5], [6], [12], where three distinct vectors adjacent to the reference vector are used to synthesize the reference vector over the carrier cycle. Let these nearest three vectors be $\vec{m}_1$, $\vec{m}_2$, and $\vec{m}_3$. Let, $d_1$, $d_2$, and $d_3$ are the dwell times of three vectors, respectively. These dwell times can be determined after solving (5). After solving (5) and substituting $\vec{m}_{ref}$ from (4b), one can get $d_{1,2,3}$ as functions of $m_A$, $m_B$, $m_C$.

$$\begin{aligned} &\vec{m}_{ref} = d_1\vec{m}_1 + d_2\vec{m}_2 + d_3\vec{m}_3 \\ &d_1 + d_2 + d_3 = 1 \end{aligned} \tag{5}$$

Based on the position of $\vec{m}_{ref}$, $-30^\circ$ to $30^\circ$ of $\alpha - \beta$ plane (CS-1) can be divided in six subsectors, namely, $1_p, 1_q, 2_p, 2_q, 3_p, 3_q$, where the applied three nearest vectors

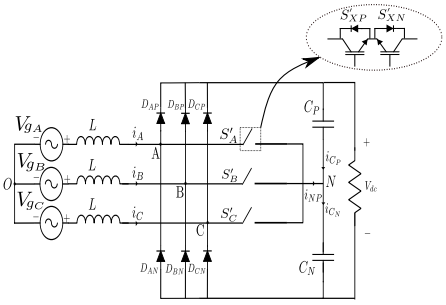

Fig. 1: 3-$\phi$ VR Circuit

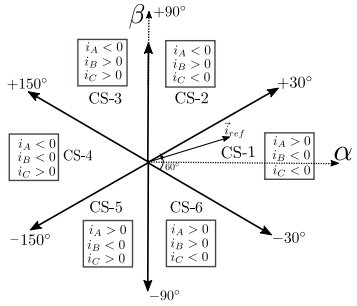

Fig. 2: current Sector Diagram

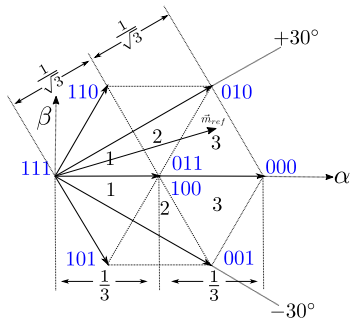

Fig. 3: Space vectors of 8 states for CS-1

are different. These subsectors are shown in Fig. 3. Note, the active vector $\frac{1}{3}e^{j0}$ is nearest to all six subsectors, hence, is common to all subsectors. And, this particular vector has two redundant states, 011 and 100. Hence, $\vec{m}_{ref}$ in each subsector can be synthesized using four switching states. These four states comprises of two redundant states corresponding to $\frac{1}{3}e^{j0}$ vector, and other two states for the other two vectors. Using these four states, the switching sequences in six subsectors are designed so that a transition from one state to another always involves transition in a single leg. These switching sequences over $T_{sw}$ are tabulated in Table II, which are mirror symmetric with respect to half period, $\frac{T_{sw}}{2}$. As the non-zero pole voltage, $v_{XN}$, is decided by the current direction in a particular leg, and current direction doesn't change over a carrier cycle, the pole voltages of VR are always unipolar. Therefore, the sequences of VR, as tabulated in Table II, are same as the sequences used by NTV modulation strategy of a three-level inverter, [5], [6].

## III. Neutral Point Voltage Unbalance in VR and the Proposed Balancing Strategy

Similar to three-level inverter, VR also suffers from voltage mismatch problem across the top and bottom DC-bus capacitors, $C_P$ and $C_N$. Ideally, the voltages across these capacitors should remain at $\frac{V_{dc}}{2}$. But these voltages drift from their ideal values due to non-zero neutral point current, $i_{NP}$, flowing out of the neutral point, $N$. This results in line current distortion and a higher voltage stress across the capacitors and devices. Fig. 4 shows the $X^{th}$ leg along with the two capacitors to illustrate the voltage unbalance problem. After applying KCL at $N$ in Fig. 4, $i_{NP}$ can be written as (6). Here, $v_{C_P}$ and $v_{C_N}$ are the voltages across $C_P$ and $C_N$; $i_{C_P}$ and $i_{C_N}$ are the currents flowing through these capacitors. Substituting $i_{C_P}$ and $i_{C_N}$ from (7) and (8) in (6), $v_{C_N}$ is shown as a function of $i_{NP}$ in (9).

$$i_{NP} = i_{C_N} - i_{C_P} \tag{6}$$

$$i_{C_P} = C_P \frac{dv_{C_P}}{dt} = -C_P \frac{dv_{C_N}}{dt} \quad (\because v_{C_P} + v_{C_N} = V_{dc}) \tag{7}$$

$$i_{C_N} = C_N \frac{dv_{C_N}}{dt} \quad (8) \quad i_{NP} = (C_P + C_N).\frac{dv_{C_N}}{dt} \quad (9)$$

From the above expressions, one can relate the rate of change of switching-cycle averaged $v_{C_N}$, denoted by $\overline{v}_{C_N}$,

TABLE II: Switching sequence of sector-1

| sub-sector | Switching Sequence |
|---|---|
| $1_p$ | 100-110-111-011-111-110-100 |
| $1_q$ | 100-101-111-011-111-101-100 |
| $2_p$ | 100-110-010-011-010-110-100 |
| $2_q$ | 100-101-001-011-001-101-100 |
| $3_p$ | 100-000-010-011-010-000-100 |
| $3_q$ | 100-000-001-011-001-000-100 |

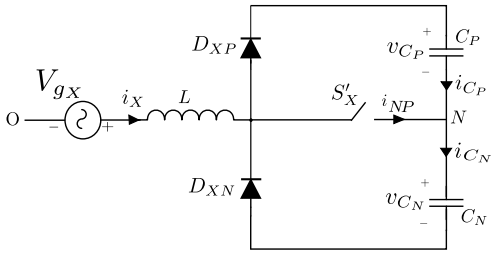

Fig. 4: Single Leg of VR

with the switching-cycle averaged $i_{NP}$, denoted by $\overline{i}_{NP}$, as shown in (10). Leibniz's integral formula is used to determine differentiation under the integration.

$$\frac{d\overline{v}_{C_N}}{dt} = \frac{d}{dt}\left(\frac{1}{T_{sw}}\int_0^{T_{sw}} v_{C_N}(\tau)d\tau\right) = \frac{1}{T_{sw}}\int_0^{T_{sw}} \frac{dv_{C_N}}{dt}d\tau$$
$$= \frac{1}{(C_P+C_N)}\underbrace{\left(\frac{1}{T_{sw}}\int_0^{T_{sw}} i_{NP}(\tau)d\tau\right)}_{\overline{i}_{NP}} = \frac{\overline{i}_{NP}}{(C_P+C_N)} \tag{10}$$

Equation (10) clearly shows that the rate of change of $\overline{v}_{C_N}$ is directly proportional to the $\overline{i}_{NP}$. Therefore, non-zero $\overline{i}_{NP}$ always results in $\overline{v}_{C_N}$ to drift from its ideal value, i.e., $\frac{V_{dc}}{2}$.

[6], [13], showed that the distribution of dwell time of the active vector between its redundant states impacts $\overline{i}_{NP}$ of three-level inverter. Same is true for VR also. To explain this, let us consider a case where $\vec{m}_{ref}$ lies in subsector 3 of CS-1 (refer Fig. 3). The nearest three vectors of subsector 3 are $\frac{2}{3}\angle 0°(\vec{m}_1)$, $\frac{1}{\sqrt{3}}\angle 30°(\vec{m}_2)$, $\frac{1}{3}\angle 0°(\vec{m}_3)$. These vectors can be implemented using 000 state (for $\vec{m}_1$), 010 (for $\vec{m}_2$), and the redundant 011 and 100 states (for $\vec{m}_3$).

Let, $d_1, d_2, d_3$ are the dwell times of three vectors, respectively. And, 011 and 100 states are applied for $xd_3$ and $(1-x)d_3$, where $x$ is a fraction between 0 and 1 and it denotes the dwell-time distribution factor between the redundant states. $i_{NP}$ corresponding to each state can be found from the following equation, where $G_X$ is defined in (1c).

$$i_{NP} = \sum_{X=A,B,C} G_X i_X \tag{11}$$

Table III lists $i_{NP}$ for the four switching states used to synthesize $\vec{m}_{ref}$ in subsector 3. Note, $i_A + i_B + i_C = 0$. The average $i_{NP}$ over $T_{sw}$, $\overline{i}_{NP}$, is given in (12a). After solving (5) $d_2$ and $d_3$ are obtained as $d_2 = 2(m_B - m_C)$, $d_3 = 2(m_C - m_A + 1)$, which are substituted to get the final expression of (12a). By rearranging, We can obtain x as a function of $\overline{i}_{NP}$ as given in (12b). Similar exercise is performed for other subsectors of CS-1 to find $x$ as function of $\overline{i}_{NP}$. Table IV tabulates these expressions for six subsectors of CS-1.

TABLE III: $i_{NP}$ for each state of subsector $3_p$

| State | $\mathbf{i_{NP}}$ | State | $\mathbf{i_{NP}}$ |
|---|---|---|---|
| 000 | 0 | 011 | $-i_A$ |
| 010 | $i_B$ | 100 | $i_A$ |

$$\begin{aligned}\bar{i}_{NP} &= 0\times d_1 + i_B\times d_2 + (-i_A)\times x d_3 + i_A\times(1-x)d_3 \\ &= (1-2x)d_3 i_A + d_2 i_B \\ &= 2(1-2x)(m_C - m_A + 1)i_A + 2(m_B - m_C)i_B \end{aligned} \tag{12a}$$

$$x = 0.5.(1 - \frac{2(m_C - m_B)i_B + \bar{i}_{NP}}{(2-2(m_A - m_C))i_A}) \tag{12b}$$

Conventional NTV (CNTV) scheme of three-level inverter or VR uses $x = 0.5$, i.e., it uses the redundant states for equal duration of time. But it will cause non-zero $\bar{i}_{NP}$, which is evident from (12a) and Table III, which has a predominant third harmonic component over the line cycle. This also results in third harmonic ripple across the capacitor voltage, [8].

As $\bar{i}_{NP}$ can be varied using $x$, which in turn can change $\overline{v}_{C_N}$, (10), [11] directly used $x$ as the control parameter to maintain $\overline{v}_{C_P}$ and $\overline{v}_{C_N}$ at $\frac{V_{dc}}{2}$ dynamically. But the large signal model of $\overline{v}_{C_N}$ to $x$ is non-linear, [11]. Therefore, the non-linear plant is linearized across an equilibrium point to obtain a small-signal transfer function $\frac{\overline{v}_{C_N}(s)}{x(s)} = \frac{G_p}{s}$. Here, $G_p$ is function of the load power factor and the magnitude of $\vec{m}_{ref}$. This control scheme reduced the magnitude of third-harmonic voltage ripple compared to conventional NTV scheme with $x = 0.5$, [11]. But it was not possible to completely eliminate the ripple, which otherwise possible theoretically by changing $x$ on a cycle-by-cycle basis [14], mainly because of the control strategy is designed on the approximated non-linear plant. It is also difficult to design controller for a plant, whose model ($G_p$) changes from one operating point to another.

This paper solves the above problems by proposing an alternative control architecture. Note the plant model of $\overline{v}_{C_N}$ to $\bar{i}_{NP}$ is derived in (10) from where one can write the large-signal transfer function as,

$$\frac{\overline{v}_{C_N}(s)}{\bar{i}_{NP}(s)} = \frac{1}{s(C_P + C_N)} \tag{13}$$

Therefore, if $\bar{i}_{NP}$ is used as control variable instead of $x$, the plant model becomes linear, large-signal valid, exact and operating point independent. One can design the neutral-point voltage balancing controller based on this plant model, whose objectives are as follows.

- Any DC offset in $v_{C_N}$ during start-up or transient should be made zero so that $\overline{v}_{C_N} = \frac{Vdc}{2}$ can be maintained.
- The third harmonic ripple voltage appeared across $v_{C_N}$, denoted by $\tilde{v}_{C_N}$, should also be made zero.

To mitigate the third harmonic ripple voltage, i.e., to make $\tilde{v}_{C_N} = 0$, the controller bandwidth should be much higher than 150 Hz (for line frequency 50 Hz). But the control of DC voltage of $v_{C_N}$ can't happen faster than the outer DC-bus voltage control of VR.

TABLE IV: Expressions of $x$ for all sub sectors in CS-1

| sub sector | x |
|---|---|
| $(\mathbf{1_p}, \mathbf{1_q})$ | $0.5.(1 - \frac{2(m_B - m_C)i_C + \bar{i}_{NP}}{2(m_A - m_B)i_A})$ |
| $(\mathbf{2_p}, \mathbf{2_q})$ | $0.5.(1 - \frac{(1-2(m_A - m_B))i_C + (1-2(m_A - m_C))i_B + \bar{i}_{NP}}{(1-2(m_B - m_C))i_A})$ |
| $(\mathbf{3_p}, \mathbf{3_q})$ | $0.5.(1 - \frac{2(m_C - m_B)i_B + \bar{i}_{NP}}{(2-2(m_A - m_C))i_A})$ |

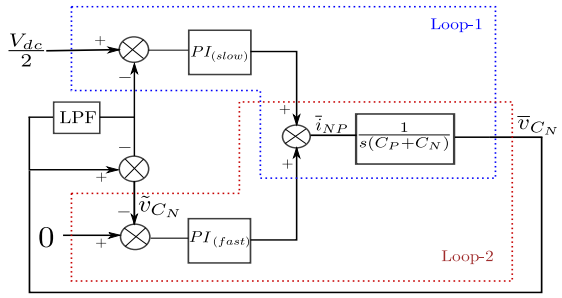


Fig. 5: Proposed closed-loop control strategy for neutral-point voltage balancing.

Let's consider an example of the converter with switching frequency, $F_{sw} = \frac{1}{T_{sw}}$, as 20 kHz. The bandwidths of the inner current and outer DC-bus voltage controllers of grid-connected VR are, suppose, 2 kHz and 200 Hz, respectively. The inner current and outer DC-bus voltage control loops are not shown here, but can be referred from [13]. Therefore, DC offset correction loop of $v_{C_N}$ can't have bandwidth higher than 200 Hz, but the same loop can't be used to mitigate third harmonic ripple voltage.

Therefore, the proposed control architecture has two loops with two different bandwidths, as shown in Fig. 5. The PI controller of the DC correcting loop, labeled as Loop-1, is designed to match the bandwidth with the outer DC voltage controller of VR. The cut-off frequency of low-pass filter (LPF) of Fig. 5 can be kept smaller than 15 Hz ($\frac{1}{10}$th of 150 Hz) to get only DC part. The ripple voltage is obtained after subtracting the LPF output from the sensed $v_{C_N}$. The second PI controller with higher bandwidth takes this ripple voltage feedback and compare with zero reference. This is labeled as Loop-2 in Fig. 5. The carrier-cycle average $\bar{i}_{NP}$ is the summation of the outputs of these two controllers. This $\bar{i}_{NP}$ is applied by changing $x$ in the modulation strategy, as discussed in the next section.

## IV. Implementation of Proposed Control Strategy

$\bar{i}_{NP}$ has an algebraic relation with $x$, as it is evident from Table IV for CS-1 operation. Similar expression, i.e., $x = f(\bar{i}_{NP}, m_A, m_B, m_C, i_A, i_B, i_C)$, can also be found for all current sectors. It was found that the expressions in six current sectors can be generalized in terms of $m_{\text{max}}$, $m_{\text{mid}}$, $m_{\text{min}}$, and $i_{\text{max}}$, $i_{\text{mid}}$, $i_{\text{min}}$, as given in Table V. The definitions of these variables are given in (14) and (15). Note, $m_{\text{mid}} = -(m_{\text{max}} + m_{\text{min}})$ and $i_{\text{mid}} = -(i_{\text{max}} + i_{\text{min}})$.

$$m_{\text{max}} = \max(m_A, m_B, m_C), \quad m_{\text{min}} = \min(m_A, m_B, m_C) \tag{14}$$

$$i_{\text{max}} = \begin{cases} i_A & m_{\text{max}} = m_A \\ i_B & m_{\text{max}} = m_B \\ i_C & m_{\text{max}} = m_C \end{cases} \tag{15a}$$

$$i_{\text{min}} = \begin{cases} i_A & m_{\text{min}} = m_A \\ i_B & m_{\text{min}} = m_B \\ i_C & m_{\text{min}} = m_C \end{cases} \tag{15b}$$

Once $\bar{i}_{NP}$ is known from the neutral-point voltage balancing strategy of Fig. 5, one can find $x$ using Table V. Note that x should be in the range $0 < x < 1$ and one should saturate x to the closest limit if it is outside this range. With this $x$, the common-mode signal, $m_{cm}$, of the three-level converter or VR can be found using (16), [13].

$$m_{cm} = x(0.5 + M_{max} - M_{min}) - M_{min} \tag{16a}$$

TABLE V: Expressions of x in all current sectors

| sub sector | x (CS-1,CS-3,CS-5) | x (CS-2,CS-4,CS-6) |
|---|---|---|
| $(\mathbf{1_p}, \mathbf{1_q})$ | $0.5.(1 - \frac{2(m_{mid}-m_{min})i_{min}+\bar{i}_{NP}}{2(m_{max}-m_{mid})i_{max}})$ | $0.5.(1 + \frac{2(m_{max}-m_{mid})i_{max}+\bar{i}_{NP}}{2(m_{mid}-m_{min})i_{min}})$ |
| $(\mathbf{2_p}, \mathbf{2_q})$ | $0.5.(1 - \frac{(1-2(m_{max}-m_{mid}))i_{min}+(1-2(m_{max}-m_{min}))i_{mid}+\bar{i}_{NP}}{(1-2(m_{mid}-m_{min}))i_{max}})$ | $0.5.(1 + \frac{(1-2(m_{mid}-m_{min}))i_{max}+(1-2(m_{max}-m_{min}))i_{mid}+\bar{i}_{NP}}{(1-2(m_{max}-m_{mid}))i_{min}})$ |
| $(\mathbf{3_p}, \mathbf{3_q})$ | $0.5.(1 - \frac{2(m_{min}-m_{mid})i_{mid}+\bar{i}_{NP}}{(2-2(m_{max}-m_{min}))i_{max}})$ | $0.5.(1 + \frac{2(m_{mid}-m_{max})i_{mid}+\bar{i}_{NP}}{(2-2(m_{max}-m_{min}))i_{min}})$ |

$$M_{max} = \max(M_A, M_B, M_C), \;\; M_{min} = \min(M_A, M_B, M_C) \tag{16b}$$

$$M_X = \begin{cases} m_X & ; m_X \geq 0 \\ m_X + 0.5 & ; m_X < 0 \end{cases} \quad \forall X \in \{A, B, C\} \tag{16c}$$

It can be shown that the duty ratios of $S'_{XP}$ and $S'_{XN}$ switches of Fig. 1, denoted by $d'_{XP}$ and $d'_{XN}$, can be determined as (17), which uses the above $m_{cm}$ signal.

$$d'_{XP} = \begin{cases} 1 - m^*_X; m^*_X \geq 0 \\ 1; \quad \text{Otherwise} \end{cases} \quad d'_{XN} = \begin{cases} 1; m^*_X \geq 0 \\ 1 + m^*_X; \quad \text{Otherwise} \end{cases} \tag{17}$$

where, $m^*_X = 2(m_X + m_{cm})$.

$d'_{XP}$ signals of all three legs are compared with one carrier signal to generate the gating signals of $S'_{XP}$, $X \in \{A, B, C\}$. On the other hand, $d'_{XN}$ signals are compared with $180°$ phase shifted carrier to generate gating signals of $S'_{XN}$, as elaborated in [6].

## V. Simulation and Experimental Validation

The proposed strategy is validated through simulation and experiment performed on a hardware setup shown in Fig. 6. The VR is made of 1200 V discrete IGBT, IKW40N120H3, and its anti-parallel diodes are used as $D_{XP}$ and $D_{XN}$ of Fig. 1. Texas Instrument's delfino series launchpad, TMS28379D, is used for digital implementation, control, and sensing. A simulation model is designed in MATLAB Simulink to verify the functionality of the proposed control. The operating conditions for the experiment are listed in Table VI.

Fig. 7a shows the experimental results for phase-locked-loop (PLL) output, i.e., grid angle $\theta$, which is synchronized with input voltage $v_{AO}$. Note $v_{AO}$, and $i_A$ are in same phase, i.e., unity power-factor operation of VR is verified. Fig. 7b and 7c show simulated waveforms of $v_{AN}$, $V_{dc}$, $v_{C_N}$ over the line cycle for CNTV strategy and our proposed control strategy, respectively. The voltage ripples across top and bottom capacitors are zoomed in Fig. 7d and 7e for these two strategies. As can be seen, $v_{C_P}$ and $v_{C_N}$ has low-frequency voltage ripples with CNTV strategy, which are equal in magnitude (12 V) but opposite in phase. The proposed controller eliminates the low-frequency ripple and high-frequency ripple voltage magnitude is reduced to 2 V, i.e., six times reduction in $\tilde{v}_{C_P}$ and $\tilde{v}_{C_N}$ is obtained. The low-frequency voltage ripple of Fig. 7d is also reflected in $v_{AN}$ envelop of Fig. 7b.

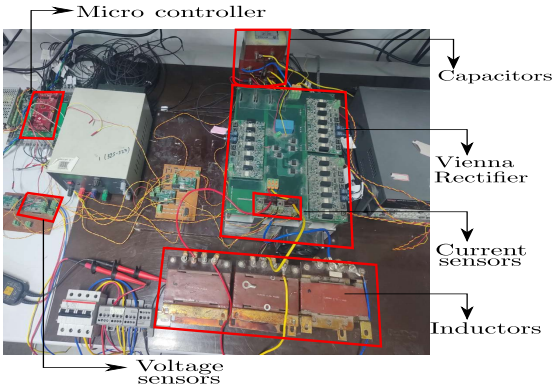


Fig. 6: Experimental set-up

TABLE VI: Operating conditions of simulation and experiments

| Quantity | Value | Quantity | Value |
|---|---|---|---|
| Input Voltage | 110 V RMS/ 50 Hz | $L$ | 7 mH |
| $C_P$, $C_N$ | 56 $\mu$F | $V_{dc}$ | 360 V |
| $F_{sw}$ | 20 kHz | $P_{out}$ | 1 kW |

Fig. 7f and 7g showcases the experimental results of pole voltage $v_{AN}$ and capacitor voltages $v_{C_P}$, and $v_{C_N}$ of CNTV strategy and our proposed strategy under non-zero DC-offset condition. Equal distribution of redundant states, i.e., CNTV, couldn't achieve neutral point DC-offset balance, as seen in Fig. 7f. But there is no DC-voltage unbalance with the proposed $\bar{i}_{NP}$ control strategy, Fig. 7g. This neutral point voltage unbalance also impacts the line-current distortion. This is evident from phase current waveforms of $i_A$ and $i_B$ given in Fig. 7h, 7i for these two strategies. The reduction of harmonic distortion achieved by the proposed strategy, Fig. 7i, compared to CNTV strategy, Fig. 7h, is clearly visible.

## VI. Conclusion

This paper proposes a two-loop control strategy for balancing the neutral point voltage of Vienna rectifier-the fast loop works on the third-harmonic ripple and the slower loop eliminates the initial or transient dc bias. This closed loop strategy gives the required neutral point current for the voltage balancing. This current can be expressed as the function of dwell-time distribution factor of one redundant state and the maximum, middle, minimum values of $3\phi$ reference signals and phase currents. A carrier-based implementation is shown to vary this distribution factor in order to vary $\bar{i}_{NP}$. With this implementation strategy, duty ratios of the switches are determined, which are compared with two $180°$ phase-shifted triangular carrier waves to generate switching pulses. The effectiveness of this strategy has been validated through simulation and experiment on a 1 kW hardware prototype, where six times neutral point voltage reduction is achieved.

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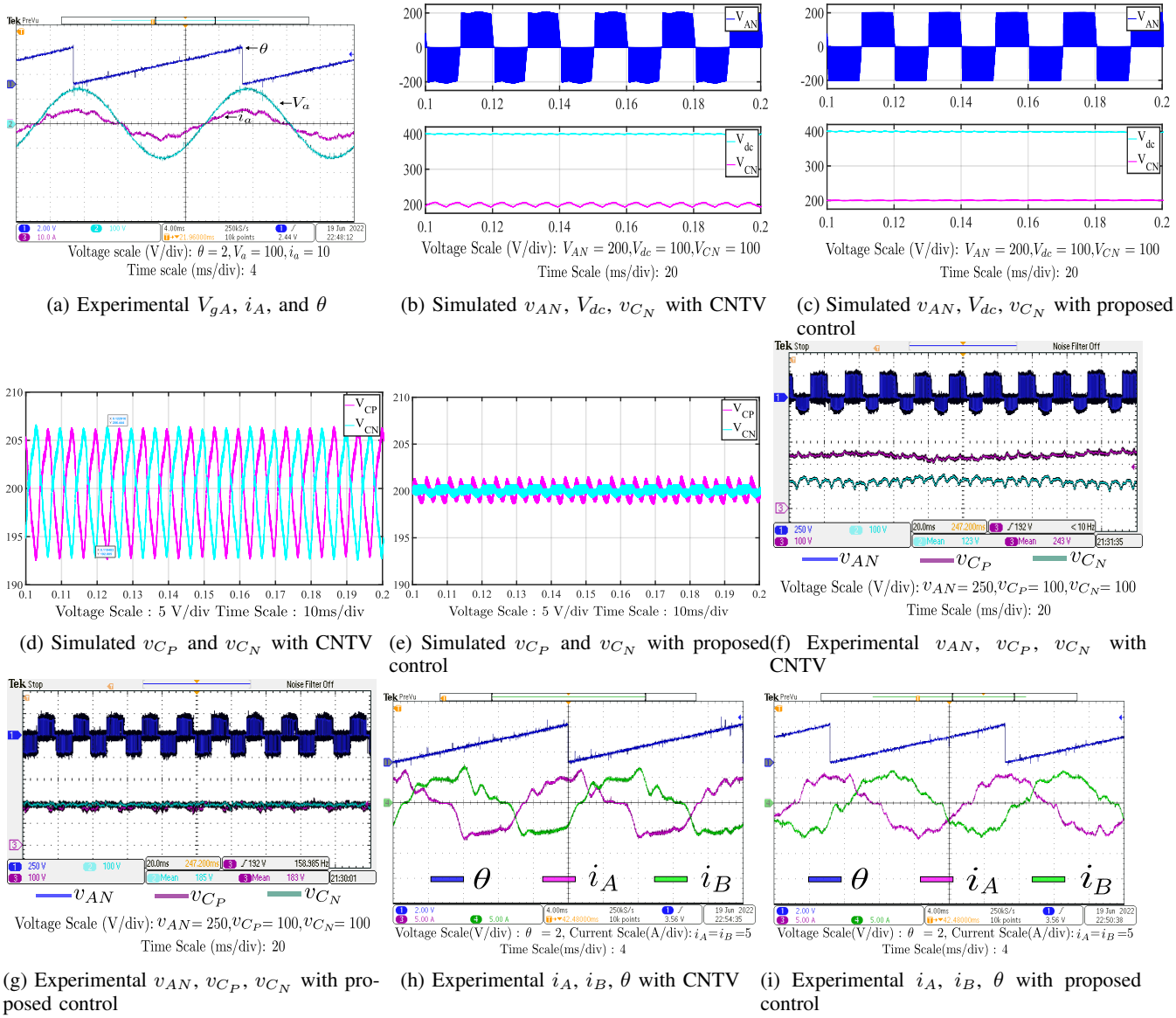


(a) Experimental $V_{gA}$, $i_A$, and $\theta$

(b) Simulated $v_{AN}$, $V_{dc}$, $v_{C_N}$ with CNTV

(c) Simulated $v_{AN}$, $V_{dc}$, $v_{C_N}$ with proposed control

(d) Simulated $v_{C_P}$ and $v_{C_N}$ with CNTV

(e) Simulated $v_{C_P}$ and $v_{C_N}$ with proposed control

(f) Experimental $v_{AN}$, $v_{C_P}$, $v_{C_N}$ with CNTV

(g) Experimental $v_{AN}$, $v_{C_P}$, $v_{C_N}$ with proposed control

(h) Experimental $i_A$, $i_B$, $\theta$ with CNTV

(i) Experimental $i_A$, $i_B$, $\theta$ with proposed control

Fig. 7: Simulation and experimental results to validate the proposed control strategy


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